

Figure 4C

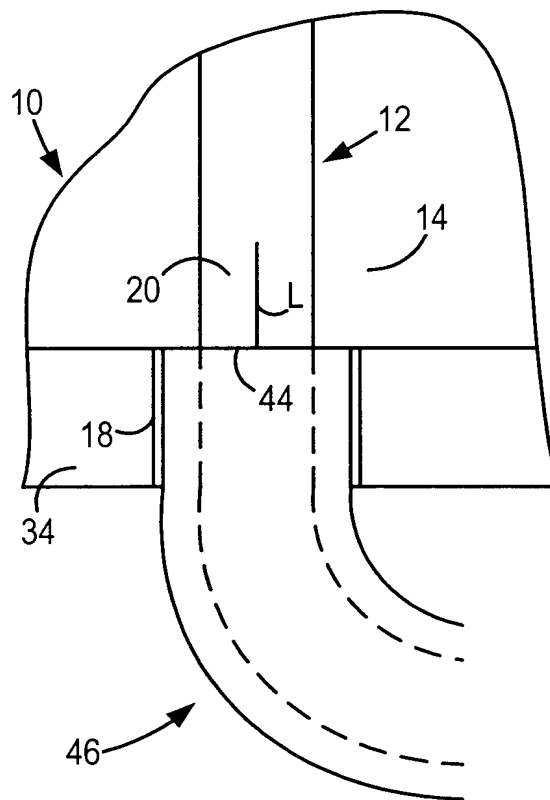


Figure 4D

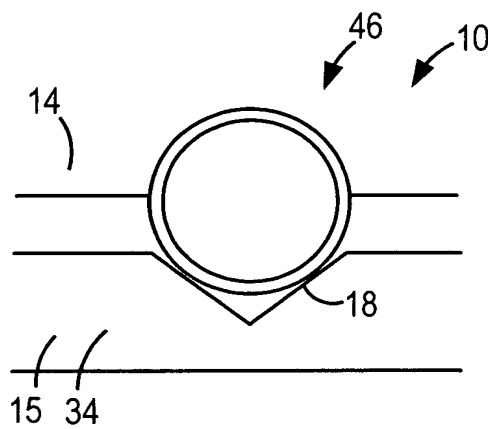


Figure 4E

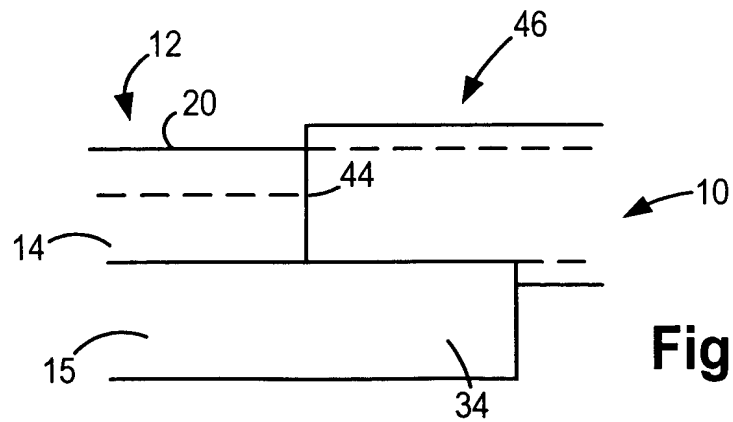


Figure 4F

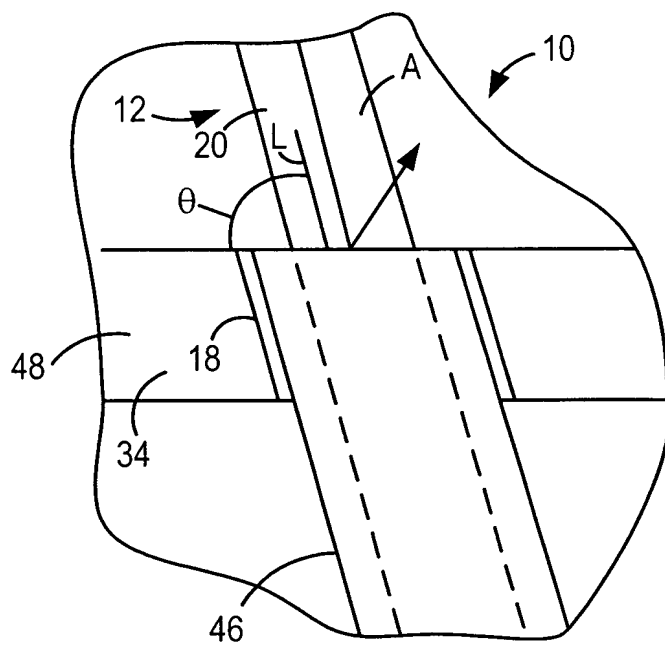


Figure 4G

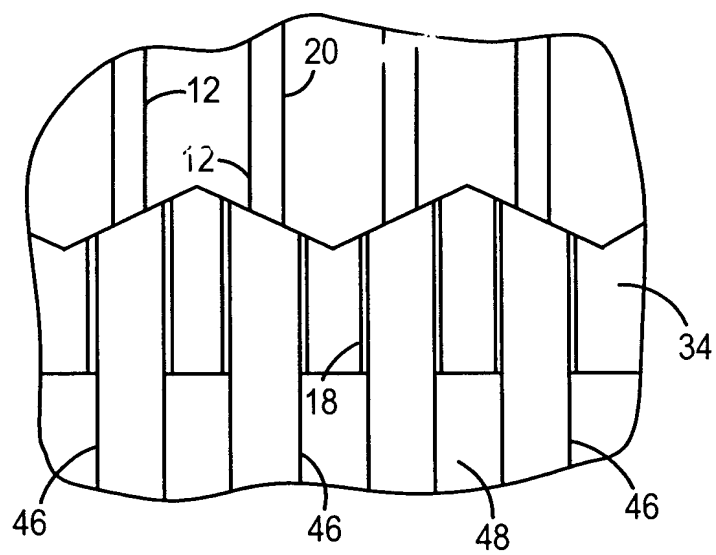


Figure 4H

Figure 5A

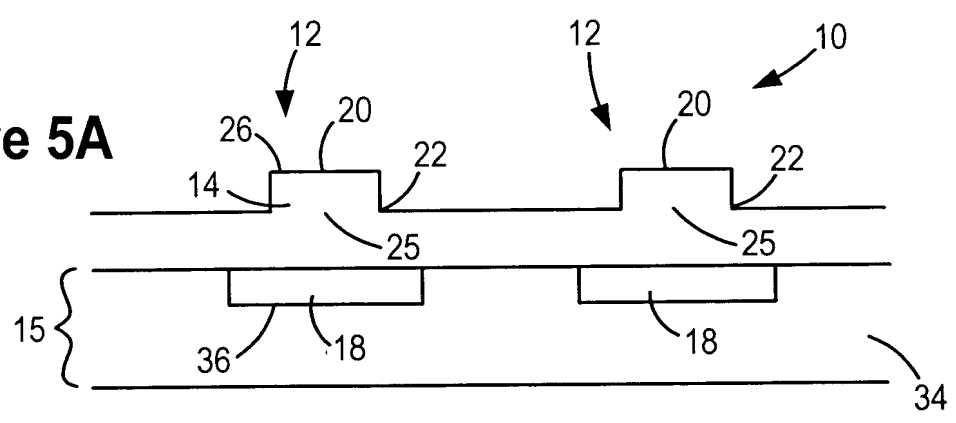


Figure 5B

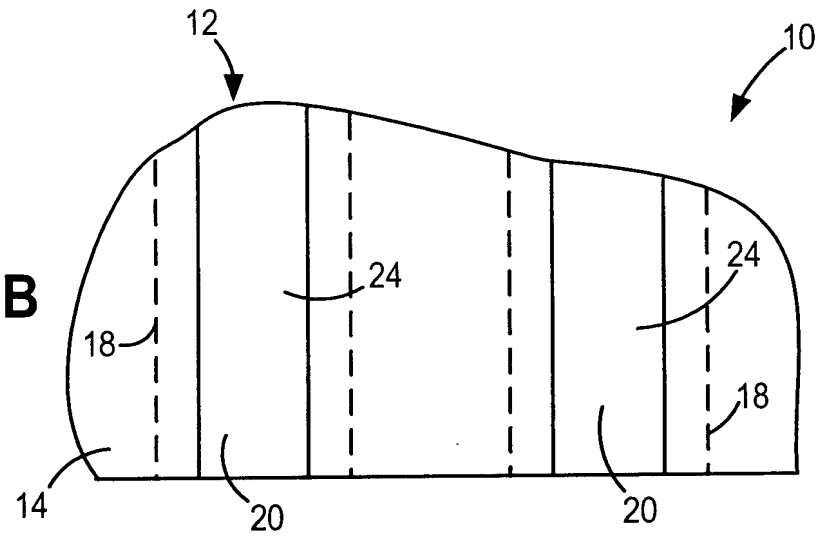


Figure 5C

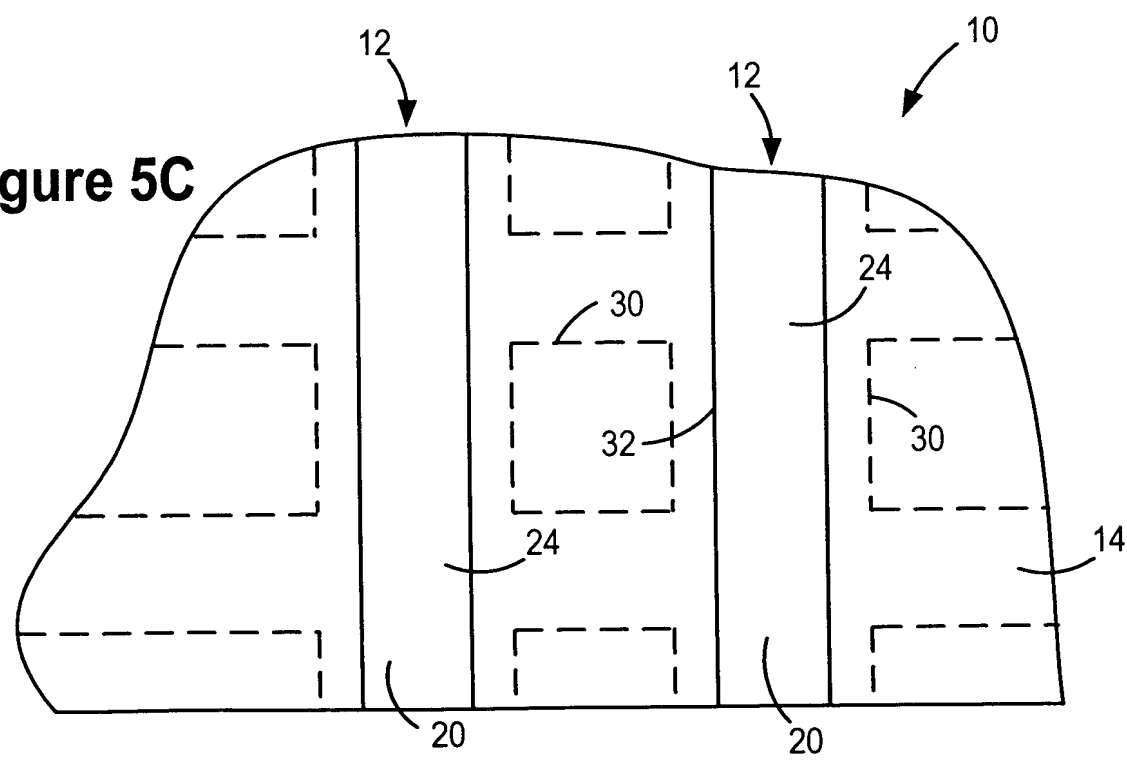


Figure 6A

Figure 6A is a cross-sectional view of a semiconductor device 10, showing a top surface 12 and a substrate 14. The device includes a gate stack 18, a gate dielectric 20, a gate electrode 24, a channel region 25, a source region 36, and a drain region 40. The gate stack 18 is formed on the substrate 14, and the gate dielectric 20 is formed on the gate stack 18. The gate electrode 24 is formed on the gate dielectric 20. The channel region 25 is formed in the substrate 14, and the source region 36 and drain region 40 are formed in the substrate 14. The substrate 14 is shown with a cross-section 15. The angle θ is indicated between the top surface 12 and the side surface of the gate stack 18.

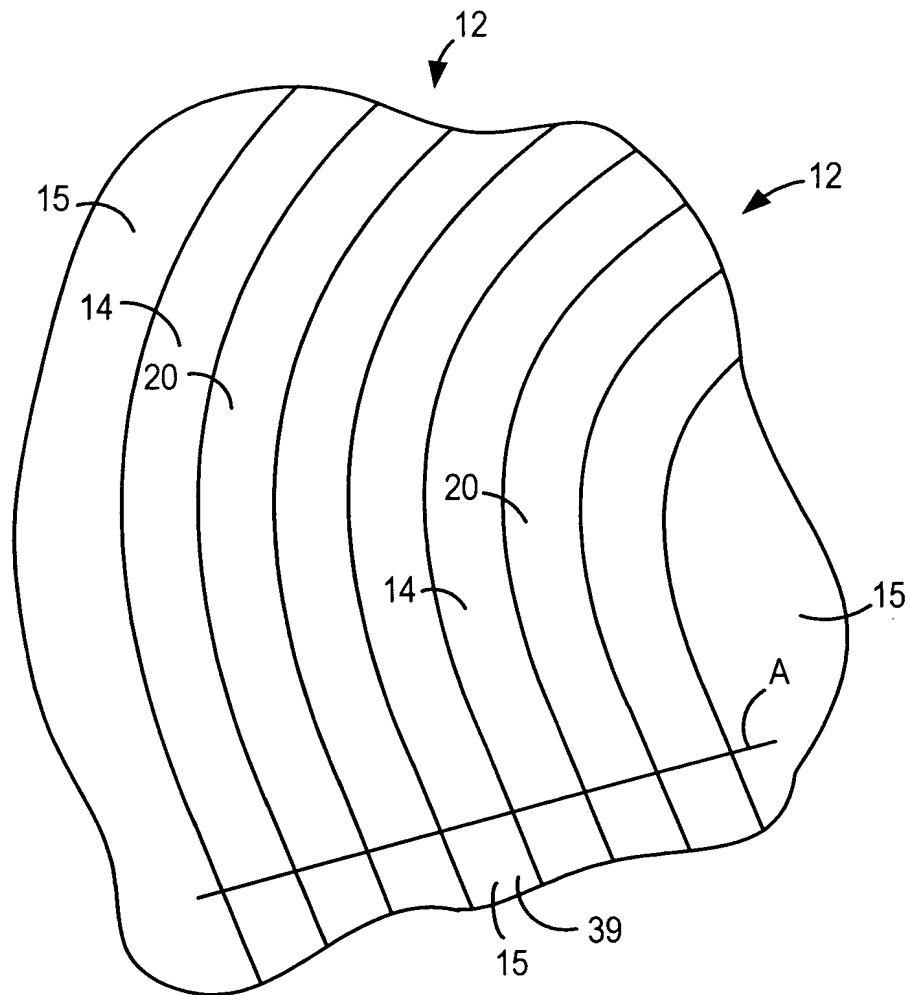


Figure 6B

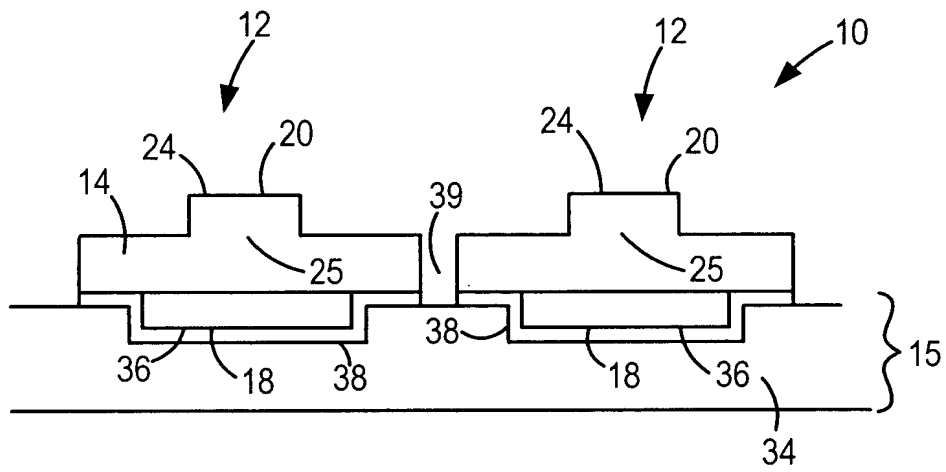


Figure 6C

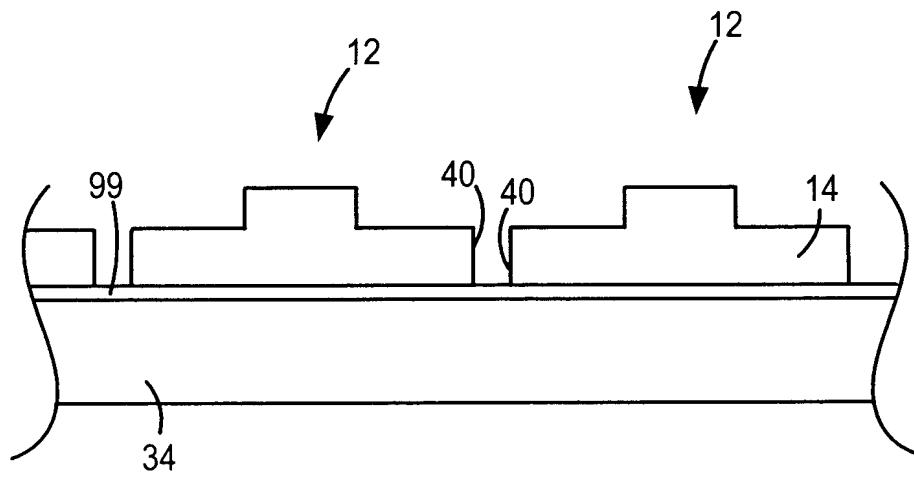


Figure 6D

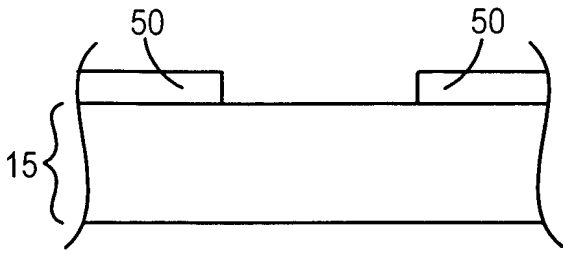


Figure 7A

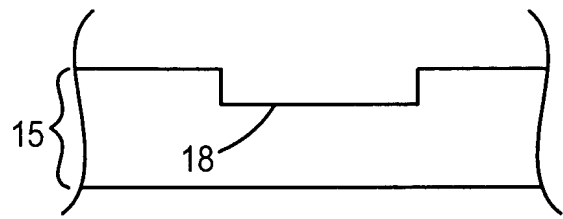


Figure 7B

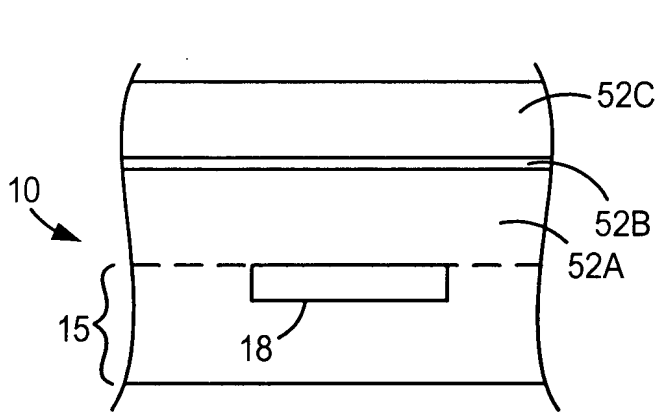


Figure 7C

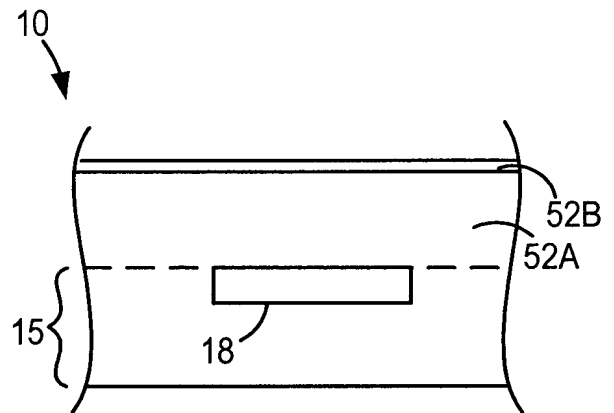


Figure 7D

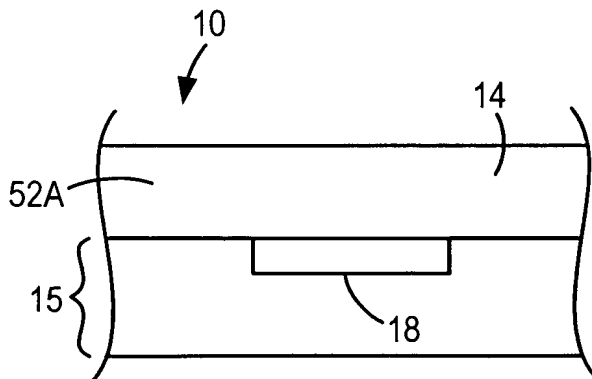


Figure 7E

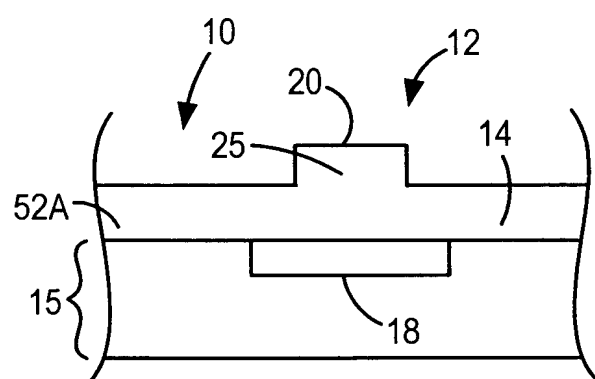


Figure 7F

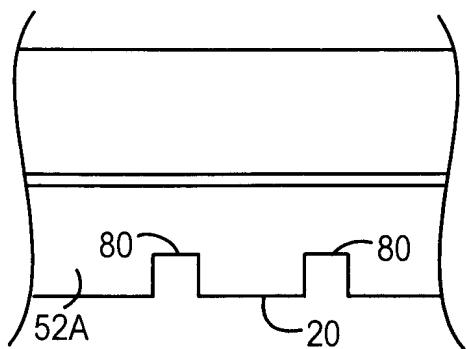


Figure 8A

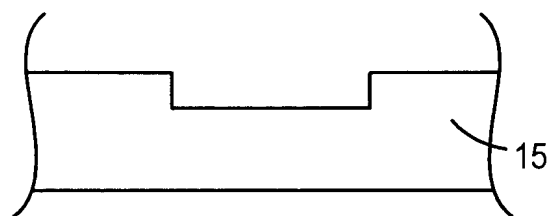


Figure 8B

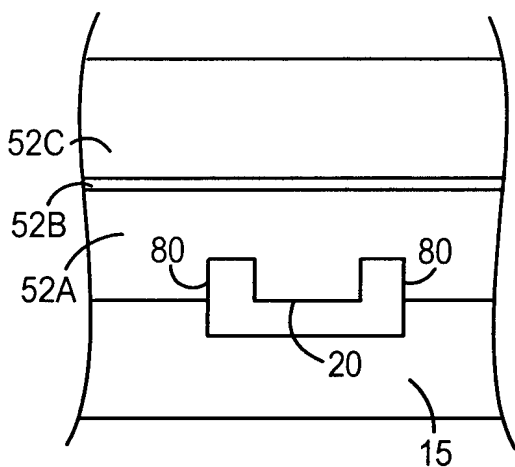


Figure 8C

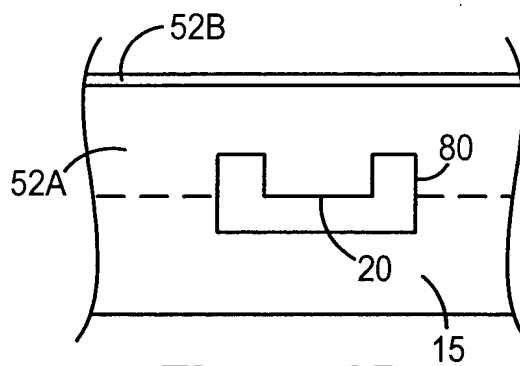


Figure 8D

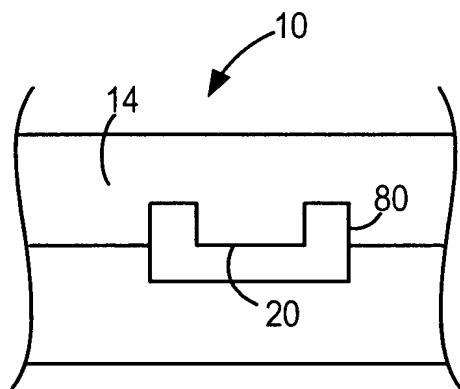


Figure 8E

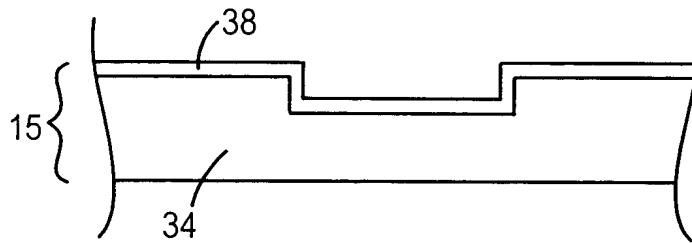


Figure 9A

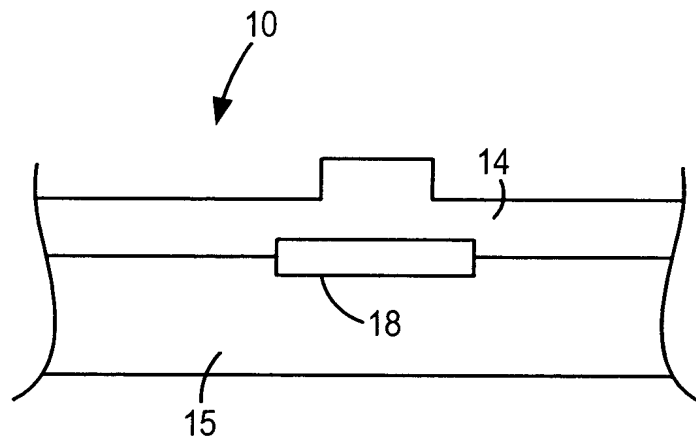


Figure 9B